Attorney's Docket No.:10559-108001
Assignee: Intel Corporation

Remarks

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1, 11-13, and 20 have been amended to correct minor typographical informalities. Claims 1, 8, and 20 have been amended to clarify that the first layer defines a non-grounded gap between said first and second portions of the first and second lines as supported by, e.g., FIG. 3. Claims 4-6, 11-13, and 16-19 have been amended to use terminology consistent with their respective independent claims. Claim 8 has been amended to relate to a method for use in routing signals. Claim 14 has been amended to address the Examiner's objection. Claims 1, 3-8, 10-14, 16-20, 23 and 24 remain pending in the application. Claims 1, 8, 14, and 20 are in independent form.

In the action mailed May 28, 2003, claim 20 was rejected under 35 U.S.C. §112, 2nd paragraph as indefinite. Claims 5, 6, 12, 13, 18, 19, and 20 have been amended to recite a perpendicular distance separating the substantially parallel second portions of the first and second signal lines, as supported by, e.g., FIG. 3.

Independent claims 1 and 20 were rejected under 35 U.S.C. §103(a) as obvious over the admitted prior art and Perino et al. (U.S. Patent No. 6,160,716, hereinafter "Perino").

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These rejections are respectfully traversed. In summary, the rejection attempts to modify the admitted prior art using exactly what Perino says not to do.

Claim 1 relates to a computer system that includes a circuit board. The circuit board includes a first signal line and a second signal line both formed on a first layer of the circuit board and both connected to a first pin on a memory unit. A first portion of the second signal line is at an acute angle relative to a first portion of the first signal line. A second portion of the second signal line is substantially parallel to a second portion of the first signal line. The first layer defines a non-grounded gap between the first and second portions of the first and second lines.

Claim 20 relates to a circuit board that includes a data bus connecting a memory control unit to a memory unit. The data bus includes a first signal line and a second signal line both formed on a first layer of the circuit board and both connected to a first pin on a memory unit. A first portion of the second signal line is at an acute angle relative to a first portion of the first signal line. A second portion of the second signal line is substantially parallel to a second portion of the first signal line. The first layer defines a non-grounded gap between the first and second portions of the first and second lines.

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In rejecting claims 1 and 20, the Office action contends that since FIG. 8 of Perino shows parallel signal lines that are separated by a non-grounded gap it would have been obvious to modify the signal lines in the admitted prior art to be parallel and separated by a non-grounded gap.

Applicant respectfully disagrees.

First, the parallel signal lines shown throughout Perino are connected to different pins on two connectors, rather than to a single first pin as in claims 1 and 20. See, e.g., FIGS. 4, 7, 11, and 16 of Perino. Indeed, connecting Perino's parallel signal lines to a single first pin will destroy the efficacy of Perino's device. See, e.g., FIGS. 4, 7, 11, and 16 and col. 2, lines 15-22 where Perino describes that connections between Perino's parallel signal lines are fabrication defects and that each signal line is to be routed around the pins to which the other signal line is connected. Perino thus fails to describe or suggest first and second signal lines both connected to a first pin on a memory unit and having substantially parallel second portions, as per claims 1 and 20.

Secondly, Perino explicitly teaches away from separating second portions of signal lines by a non-grounded gap. Attention is respectfully directed to FIG. 11 and the written description thereof, where Perino describes the advantages of

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ground traces 1160 in preventing signal interference between unconnected signal lines 1170. Since Perino explicitly teaches away from the separating as claimed, any combination involving Perino is improper.

Finally, the impedance mismatch referred to in page 4-5 on the Office action arises due to the high impedance of signal lines that are relatively narrow to accommodate "two-between" routing (i.e., routing two signal lines between two other pins such as two ground pins). See, e.g., col. 2, lines 15-33 of Perino. Such two-between routing is illustrated in FIG. 8 of Perino which was relied upon in rejecting claims 1 and 20. Thus, according to Perino, the teachings relied upon in rejecting claims 1 and 20 are disadvantageous. It is therefore respectfully submitted that one of ordinary skill in the art would find no suggestion to combine Perino with the admitted prior art in the manner suggested.

Since there is no suggestion to combine Perino with the admitted prior art and Perino fails to describe or suggest first and second signal lines both connected to a first pin on a memory unit and having substantially parallel second portions, it is respectfully submitted that a *prima facie* case of obviousness has not been established. Furthermore, since Perino explicitly teaches away from the claimed invention, it is

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respectfully submitted that any combination involving Perino is improper and would not be attempted by one having ordinary skill. Accordingly, Applicant submits that claims 1 and 20, and the claims dependent therefrom, are allowable.

Independent claim 8 was rejected under 35 U.S.C. §103(a) as obvious over the admitted prior art and Perino.

This rejection is respectfully traversed.

Claim 8 relates to a method including delivering a first signal over a first signal line connected to a first pin on a memory unit and delivering a second signal over a second signal line connected to the first pin of the memory unit. A first portion of the second signal line is formed at an acute angle relative to a first portion of the first signal line. A second portion of the second signal line is formed substantially parallel to a second portion of the first signal line. The first and second portions of the first and second signal lines are separated without a ground connection therebetween.

As discussed above, Perino fails to describe or suggest first and second signal lines both connected to a first pin on a memory unit and having substantially parallel second portions and therefore fails to describe or suggest delivering signals over such lines. Further, Perino explicitly teaches away from separating signal lines without a ground connection

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therebetween. Finally, according to Perino, the teachings relied upon in rejecting claim 8 are disadvantageous, and hence there is no suggestion to combine the references in the suggested manner.

It is therefore respectfully submitted that a *prima facie* case of obviousness has not been established and that the suggested combination is improper. Accordingly, Applicant submits that claim 8 and the claims dependent therefrom are allowable.

Independent claim 14 was rejected under 35 U.S.C. §103(a) as obvious over the admitted prior art and Perino.

This rejection is respectfully traversed.

Claim 14 relates to a method that includes connecting a memory unit to the board such that a first pin on the memory unit connects to first and second signal lines, forming a first portion of the second signal line to be at an acute angle relative to a first portion of the first signal line, and forming a second portion of the second signal line to be substantially parallel to a second portion of the first signal line.

As discussed above, Perino fails to describe or suggest first and second signal lines both connected to a first pin on a memory unit and having substantially parallel second portions

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and therefore fails to describe or suggest forming such signal lines. Further, according to Perino, the teachings relied upon in rejecting claim 14 are disadvantageous, and hence there is no suggestion to combine the references in the suggested manner.

It is therefore respectfully submitted that a *prima facie* case of obviousness has not been established. Accordingly, Applicant submits that claim 14 and the claims dependent therefrom are allowable.

In view of the above remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/24/03

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